ECE380 – Digital Logic
ABET Syllabus

Catalog Data: ECE 380: Digital Logic. Four (4) credit hours. Number systems; Boolean algebra; logic functions and gates; design of combinational logic systems; flip-flops; design of synchronous sequential systems; and iterative networks. Includes lab experiments.

Prerequisite: ECE 285 or CS 150, MA 125 Prerequisite topics: knowledge of a programming language.


Contact Hours and Additional Course Information:
The course meets multiple lecture periods weekly with a total of 150 minutes of lecture contact per week and 110 minutes of lab contact per week. The course is required in the electrical engineering program and is required in the computer engineering option.

Relationship of Course Toward Meeting ABET Student Outcomes:
The course supports instruction for Student Outcomes A, B, C, E, and K as required by ABET Criterion 3 and ABET Program Criteria. The relationships are indicated in the Course Learning Objectives.

The course supports assessment for Student Outcomes A, B, E, and K as required by ABET Criterion 3 and ABET Program Criteria. The relationships are indicated in the Student Outcome Measure Assessments.

Course Learning Objectives:
The overall course objective is to teach electrical engineering, computer engineering and computer science students the fundamental concepts, methods of analysis, and design of digital logic devices and systems. At the end of this course, students are expected to be able to:

1. Develop an understanding of designing a digital logic circuit based system to achieve a prescribed task. (Outcome A)
2. Analyze and synthesize logic networks using both traditional techniques (such as K-maps and state tables) and modern CAD tools. (Outcome A)
3. Develop an ability to conduct experiments, as well as analyze and interpret data. (Outcome B)
4. Define a test procedure (including objectives and equipment set-up) to measure the characteristics of an electronic device or circuit. (Outcome B)
5. Configure, operate, and debug an experimental set-up using standard lab equipment. (Outcome B)
6. Design a system, component, or process to meet a set of specifications. (Outcome C)
7. Design, conduct, and interpret a validation test. (Outcome C)
8. Decompose a system into components. (Outcome E)
9. Describe practical engineering problems. (Outcome E)
10. Recognize the need to use modern tools to assist solving problems. (Outcome K)
11. Identify and apply appropriate modern technologies to an assigned task. (Outcome K)
12. Use modern CAD, analysis, and simulation software. (Outcome K)
13. Students gain proficiency with Altera Quartus II, a VHDL software package, and utilize this software package to solve problems on a wide-range of digital logic circuits. (Outcome K)

Student Outcome Measure Assessments:
During this course, learning assessments will be performed using specific Student Outcome Measures that demonstrate students are able to:
1. Analyze and design logic networks using both traditional techniques (such as K-maps and state tables) and modern CAD tools. (Outcome A, Measure A8)
2. Define a test procedure (including objectives and equipment set-up) to measure the characteristics of an electronic device or circuit (analog or digital). (Outcome B, Measure B1)
3. Configure, operate, and debug an experimental set-up using standard lab equipment. (Outcome B, Measure B3)
4. Decompose a relatively complicated system into simpler components. (Outcome E, Measure E1)
5. Use modern CAD, analysis, and simulation software. (Outcome K, Measure K4)

**Contribution of Course to Meeting the ABET Professional Component:**

- Skills required, used, and developed include digital logic circuit analysis and synthesis.
- Estimated Content: Engineering Science: 1.5 credits, Engineering Design: 2.5 credits

**Relationship of Course to Program Educational Objectives:**

The course supports Program Educational Objectives 1 and 2 by developing a student’s ability to understand, analyze, and design digital logic-based systems; developing a student’s appreciation of the rapid advancement in the field reinforcing the need for life-long learning.

**Topics Covered During Class:**

1. Introduction to digital systems (1 hr)
2. Number systems (5 hrs)
3. Digital Logic Circuits (6 hrs)
   a. Variables, logic gates, networks; Truth tables, Boolean Algebra
   b. Synthesis using AND, OR and NOT gates; Design examples
4. Introduction to CAD tools and VHDL (2 hrs)
5. Implementation Technology (6 hrs)
   a. Transistor switches, Logic families (TTL, CMOS); Programmable Logic Devices (PLDs)
6. Implementation of Logic Functions (7 hrs)
   a. Logic function minimization, Karnaugh maps; Minimum SOP/POS forms, don’t-care conditions
   b. Multi-output logic circuits, NAND-NAND, NOR-NOR; Multilevel synthesis and analysis
7. VHDL based logic synthesis, optimization, physical design, and timing simulation (2 hrs)
8. Arithmetic Circuits (5 hrs)
   a. Adders/subtracters, fast adders, arithmetic circuits using VHDL
9. Combinational Logic Circuit Building Blocks (7 hrs)
   a. Multiplexers, decoders, demultiplexers, encoders, comparators
10. Sequential Logic Circuit Building Blocks (6 hrs)
    a. Latches, flip-flops (SR, JK, D and T), registers, counters, VHDL storage elements and counters
11. Synchronous Sequential Logic Circuits (7 hrs)
    a. FSM design, state assignment, Mealy and Moore machines, VHDL-based FSM design
12. Synchronous Sequential Logic Circuit Analysis (2 hrs)
13. Examinations (4 hrs)
14. Final comprehensive examination (2.5 hrs)

**Laboratory:** Eight to ten laboratory projects related to the course material are performed throughout the semester.

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