ECE380 Digital Logic: Design Activity #2

Using Schematic-Based Designs and VHDL-based Designs in Altera Quartus II and Introduction to the Altera DE Board

INTRODUCTION

In Design Activity #2 you will become familiar with VHDL-based design and continue the use of schematic design using the Altera Quartus II software. The Altera U.P. Simulator will be used to perform functional and timing-based simulations for several combinatorial logic circuits. The Altera DE2 board will be used to implement the designed logic circuits.

PRE-LAB WORK

As lab work will be performed in groups in the lab, groups should work together in performing pre-lab tasks.

1. PRE-LAB TASK 1: Schematic Design-Based Multiplexer Circuit

Construct a truth table and K-map for a 2:1 multiplexer circuit. The circuit should have two data inputs (x and y), one select input (s) and one data output (f). Use the K-map to determine the minimum sum-of-products (SOP) form solution for the multiplexer circuit. Within the Altera Quartus II Schematic editor, complete the minimum SOP logic circuit that implements the 2:1 multiplexer. In the lab we will be using the Altera DE2 board to implement the circuit. Therefore, the device for your designed circuit will be the Cyclone II EP2C35F672C6. The pin assignments you should use for the signals are given in Table 2.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Pin</th>
<th>DE2 Board Component</th>
</tr>
</thead>
<tbody>
<tr>
<td>x</td>
<td>PIN_N25</td>
<td>SW[0] – slider switch 0</td>
</tr>
<tr>
<td>y</td>
<td>PIN_N26</td>
<td>SW[1] – slider switch 1</td>
</tr>
<tr>
<td>f</td>
<td>PIN_AE22</td>
<td>LEDG[0] – green LED 0</td>
</tr>
</tbody>
</table>

Compile the design using the instructions from the Quartus II Introduction (http://jjackson.eng.ua.edu/courses/ece380/assignments/Quartus_II_Introduction.pdf).

Complete both a functional- and timing-based simulation showing exhaustive testing of the multiplexer design using the Altera U.P Simulator. For each simulation case, the total simulation time should be 640 ns, allowing 80 ns of simulation time for each of the eight valuations of the three input signals (x, y and s).

Create a validation plan that describes how you will test your design when implemented on the Altera DE2 board.

TA check: As soon as you enter lab, provide the TA with a pre-lab report that includes the truth table and K-map for the circuit, the minimum SOP logic circuit implemented within the Altera Quartus II
Schematic editor and the two simulations. Make sure your group member names and date are on the report.

2. **PRE-LAB TASK 2: VHDL-Based Multiplexer Design**

Repeat the design from Task 1, creating a VHDL-based design of the 2:1 multiplexer circuit. In the lab we will be using the Altera DE2 board to implement the circuit. Therefore, the device for your designed circuit will be the Cyclone II EP2C35F672C6. The pin assignments you should use for the signals are given in Table 2.

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</tr>
<tr>
<td>y</td>
<td>PIN_N26</td>
<td>SW[1] – slider switch 1</td>
</tr>
<tr>
<td>f</td>
<td>PIN_AE23</td>
<td>LEDR[0] – red LED 0</td>
</tr>
</tbody>
</table>

Compile the design using the instructions from the Quartus II Introduction (http://jjackson.eng.ua.edu/courses/ece380/assignments/Quartus_II_Introduction.pdf).

Complete both a functional- and timing-based simulation showing exhaustive testing of the multiplexer design using the Altera U.P Simulator. For each simulation case, the total simulation time should be 640 ns, allowing 80 ns of simulation time for each of the eight valuations of the three input signals (x, y, and s).

Create a validation plan that describes how you will test your design when implemented on the Altera DE2 board.

**TA check:** As soon as you enter lab, provide the TA with a pre-lab report that includes the VHDL design for the circuit and the two simulations. Make sure your group member names and date are on the report.

**LABORATORY WORK**

During your lab period, you will test your two designs by implementing the circuits on the Altera DE2 board. Use the procedure described in section 9.0-9.1 of the Quartus II Introduction for programming and configuring your design onto the FPGA device. You will test your implementation(s) using your validation plan to verify that your designs meet the specifications. If your implementation fails to pass your validation plan, then you must discover and correct your design errors, document any changes, and eventually pass the validation test.

**TA check:** At the completion of the validation tests, you need to organize your test data, describe any corrections to your original design, and have the TA verify your results.

**LABORATORY REPORT**

By class time on Friday of the week the lab is performed, provide the class instructor a hardcopy of a lab report following the ECE380 Lab report Template given on the class website. Each lab group will submit one joint lab report.
GRADING POLICY

1. Quality and correctness of the pre-lab work (30%)
   a. 10% for neatness and presentation of the design
   b. 10% for the correctness of the design
   c. 10% for the completeness and appropriateness of the validation plan

2. Successful implementation of the design (50%)

3. Quality and correctness of the lab report and validation data (20%)
   a. 10% for the neatness and clarity of the design corrections
   b. 10% for neatness and presentation of the data