ECE380 Digital Logic: Design Activity #4

Standard Logic Chips and National Instruments ELVIS Breadboarding for Combinational Logic Circuits

INTRODUCTION

In Design Activity #4 you will use the National Instruments ELVIS to breadboard and test several standard logic chips and experimentally determine the truth table for a given circuit.

PRE-LAB WORK

As lab work will be performed in groups in the lab, groups should work together in performing pre-lab tasks.

1. PRE-LAB TASK 1: Familiarization with Standard Logic Chips and the National Instruments ELVIS

Familiarize yourself with the pin-out diagrams of the 7400, 7404, 7410, and 7420 chips. The website www.alldatasheet.com contains pin-out diagrams of all the devices we will use. Other websites may contain similar datasheets.

Read chapters 1-3 of the NI Educational Laboratory Virtual Instrumentation Suite (NI ELVIS) User Manual located at http://jjackson.eng.ua.edu/courses/ece380/assignments/. In particular, you should understand the layout of the NI ELVIS Prototyping Board, the Digital Bus Reader, and the Digital Bus Writer. The NI ELVIS Prototyping Board is shown in Figure 1 (reproduced from Figure 3-2) in the NI ELVIS User Manual.

![Figure 1. NI ELVIS Prototyping Board.](image)

The NI ELVIS environment consists of a data acquisition (DAQ) board located in the host computer, a hardware breadboarding surface for constructing circuits and interfacing experiments, and the NI ELVIS software. The NI ELVIS
software includes a set of soft front panel (SFP) instruments (i.e. DMM, oscilloscope, etc.) to aid in testing and debugging of designs. SFP instruments to be used in this course include a Digital Bus Writer, a Digital Bus Reader, a Digital Multimeter, a Function Generator, an Oscilloscope, and Variable Power Supplies.

The NI ELVIS software contains a virtual instrument launcher, shown in Figure 2, from which all the SFP instruments may be started. Use **Start->All Programs->National Instruments->NI ELVIS Traditional->NI Elvis Traditional** to start the NI ELVIS software. Report any software errors or malfunctions to the graduate teaching assistant or course instructor.

![Figure 2. National Instruments Virtual Instrument Launcher.](image)

The Digital Bus Reader shown in Figure 3 reads digital data from the NI ELVIS digital input (DI) bus. You can either continuously read from the bus or you can take a single reading. The Digital Bus Writer shown in Figure 4 updates the NI ELVIS digital output (DO) bus with user-specified digital patterns. Users can manually create a pattern or select predefined patterns, such as ramp, toggle, or walking 1s. This instrument can either continually output a pattern or just perform a single write. The output of the Digital Bus Writer stays latched until the instrument is stopped or another pattern is output.
2. PRE-LAB TASK 2: Understanding Breadboarding and Circuit Construction Guidelines

Breadboarding is a fundamental technique for the construction, test, and debugging of electronic circuits including digital systems. Circuits that are properly constructed using sound breadboarding practices can be easily tested, debugged and modified. Following basic guidelines in circuit construction can facilitate the debugging and testing process. Properly formed circuits are regular and are laid out on a breadboarding surface with testing, debugging, and ease of modification in mind. Improperly laid out circuits can be difficult to debug and even more difficult to modify. We will adopt guidelines in the construction of all circuits.

Review the breadboarding and circuit construction guidelines below and be prepared to follow these guidelines in the construction of circuits in lab.

1) All wiring and IC insertion should be done with no power applied to the breadboard. All connections should be checked before applying power to the breadboard.
2) Use a color code convention for wires in your design. Reserve red wires for power (+5V, +3.3V, etc.) and black for ground. If multiple power supplies are required, green may be used for the secondary power supply (i.e. red=+3.3V, green=+5V). Other colors (yellow, white, blue, etc.) can be used for signal wires.

3) Use only 22-24 gauge solid wire if possible. 22-24 gauge stranded wire that has been “tinned” with solder at the breadboard end may be used if necessary.

4) Wires should be cut to a desired length not longer than necessary. Stripping 1/4 to 3/8 inch of insulation from the wires and cutting the end of the wire on a 45 degree angle will allow for easy insertion into the breadboard. Push the wire as far as it will go into the breadboard to insure a good connection. Keep wires as low to the breadboard as feasible.

5) Wires should be laid out such that they never cross over an integrated circuit (IC) or component. This will facilitate removing ICs and other devices if it should be necessary to do so.

6) Breadboarding surfaces contain horizontal rows of connections that are typically used to distribute power to circuits being constructed. Use these rows to create power and ground busses for your circuit.

7) Orient all ICs in your design in the same direction on the breadboard. We will adopt the convention such that pin 1 of any DIP is located closest to the designer when looking at the NI ELVIS unit.

8) Before attempting to insert an IC into the breadboard make sure that all leads are straight. Straighten any bent pins with needle-nose pliers. For DIP (dual inline package) ICs, insert one side of the IC into the breadboard then gently insert the remaining sides. This will minimize the possibility of bending pins when inserting ICs into the breadboard.

9) Use only IC pullers to remove ICs from the breadboard. Using fingers or other objects increases the possibility of bending IC pins.

3. PRE_LAB TASK 3: Expanded Logic Diagrams

An expanded logic diagram shows individual gates, logic chip numbers and pins used on the integrated circuit for a particular logic gate. For example, Figure 5 below represents a single 2-input NAND gate, numbered gate 1, i.e. (1-1), from a 7400 device referred to in the logic diagram as chip one, i.e. (1-1), using pins 1 and 2 for the X and Y inputs and pin 3 for the output f. This labeling gives us a mechanism for numbering all integrated circuits used in a design as well as individual pins used on the device.

![Figure 5. Expanded Logic Diagram for a Single 2-input NAND Gate.](image)

Draw an expanded logic diagram for the circuit given in Figure 6 below. Determine the truth table for the circuit shown below and develop a data table for recording your experimental results in lab. The data table is a truth table for which you will fill in the value for an output function as you test all valuations of the circuit inputs.
Within the Altera Quartus II Schematic editor, enter the logic circuit exactly as shown in Figure 6. In the lab we will be using the Altera DE2 board to implement the circuit in addition to implementing the circuit on the NI ELVIS. The device for your designed circuit will be the Cyclone II EP2C35F672C6. The pin assignments you should use for the signals are given in Table 1.

Table 1. DE2 Pin Assignments for the Schematic-Based Multiplexer Circuit

<table>
<thead>
<tr>
<th>Signal</th>
<th>Pin</th>
<th>DE2 Board Component</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>PIN_N26</td>
<td>SW[1] – slider switch 1</td>
</tr>
<tr>
<td>D</td>
<td>PIN_N25</td>
<td>SW[0] – slider switch 0</td>
</tr>
<tr>
<td>f</td>
<td>PIN_AE22</td>
<td>LEDG[0] – green LED 0</td>
</tr>
</tbody>
</table>

Compile the design using the instructions from the Quartus II Introduction (http://jjackson.eng.ua.edu/courses/ece380/assignments/Quartus_II_Introduction.pdf).

Complete a timing-based simulation showing exhaustive testing of the design using the Altera U.P Simulator. For each simulation case, the total simulation time should be 1280 ns, allowing 80 ns of simulation time for each of the sixteen valuations of the four input signals.

Create a validation plan that describes how you will test your design when implemented on the Altera DE2 board.

TA check: As soon as you enter lab, provide the TA with a pre-lab report that includes the expanded logic diagram for the circuit, the logic circuit implemented within the Altera Quartus II Schematic editor and the timing simulation. Make sure your group member names and date are on the report.

LABORATORY WORK

During your lab period, you will test a 7404, 7400, and 7420 chip using the NI ELVIS Digital Bus Writer to control the inputs and the Digital Bus Reader instrument to monitor the outputs. Make sure each gate on each device functions correctly.

During your lab period, you will also test the design of your NAND-only circuit by implementing the circuit with standard logic chips. The NI ELVIS Digital Bus Writer instrument will be used to provide the data inputs for the circuit. Use signals D3 for A, D2 for B, D1 for C and D0 for D. The Digital Bus Reader instrument will be used to view the output f (using signal DI0).

You will test your implementation(s) using your validation plan to verify that your designs meet the specifications. If your implementation fails to pass your validation plan, then you must discover and correct your design errors, document any changes, and eventually pass the validation test.
TA check: At the completion of the validation tests, you need to organize your test data, describe any corrections to your original design, and have the TA verify your results.

LABORATORY REPORT

By noon on Friday of the week the lab is performed, provide the TA a hardcopy of a lab report following the ECE380 Lab report Template given on the class website. Each lab group will submit one joint lab report to the TA.

GRADING POLICY

1. Quality and correctness of the pre-lab work (30%)
   a. 10% for neatness and presentation of the design
   b. 10% for the correctness of the design
   c. 10% for the completeness and appropriateness of the validation plan
2. Successful implementation of the design (50%)
3. Quality and correctness of the lab report and validation data (20%)
   a. 10% for the neatness and clarity of the design corrections
   b. 10% for neatness and presentation of the data