

ECE 380 -- DESIGN ACTIVITY #9

Flip-Flops and Finite State Machines

1. INTRODUCTION

In this lab, you will use design and test various finite state machines (FSMs) using JK flip-flops. The requirements for this lab consist of completing designs and printing any necessary circuit diagrams, MAX+PLUSII schematic design files, simulation results and laboratory report. Include timing simulation results for the MAX EPM7128SLC-7 device.

Before you come to your lab session, you need to:

1. Familiarize yourself with the pin-out diagram of the 7476 dual JK flip-flop integrated circuit. A datasheet for this device may be found at <http://focus.ti.com/lit/ds/symlink/sn7476.pdf>.
2. Determine the state diagram, state table, state-assigned state table, excitation table and corresponding K-maps for flip-flop inputs and FSM outputs for each FSM designed. You will also develop a data table for recording your experimental results verifying the functionality of the designed FSM. The data table is a truth table for which you will fill in the value for an output function as you test valuations of the circuit inputs.
3. Draw the logic circuit for each designed FSM.
4. Create all required schematic (*.gdf) designs. (**BEFORE YOUR ASSIGNED LAB TIME**).

2. FLIP-FLOP FUNCTIONAL VERIFICATION

Using the LD-2 Pencilbox Logic Designer, verify the truth table describing the functionality of a JK flip-flop. Use switches **S0** and **S1** on the trainer for the J and K flip-flop inputs respectively. Use switches **S2** and **S3** for the PRESET and CLR inputs. Note the active low functioning of these two inputs. Use logic indicator **L0** for the flip-flop output and pulser **PB1** as the flip-flop clock.

3. DESIGN

DESIGN A: Design a FSM that functions as a sequence detector. The FSM should be capable of detecting two different input sequences $w=101$ and $w=110$. The FSM should have a single input, **w**, and an active low rest input, **RESETn**. The FSM should be capable of detecting either sequence in an overlapping fashion. Use the state assignment guidelines given in class to obtain a good state assignment for your design. Construct your design using JK flip-flops and any necessary NAND gates for combinational logic using the LD-2 Pencilbox Logic Designer. Verify the design by testing input valuations and observing the outputs.

DESIGN B: Design a FSM that functions as a 2-bit binary up/down counter. The FSM should have a single input, **U**, for controlling the count direction ($U=1$ implies an up count) and an active low rest input, **RESETn**. Implement your design using JK flip-flops and any necessary NAND gates for combinational logic. Construct your using the LD-2 Pencilbox Logic Designer. Verify the design by testing input valuations and observing the outputs.

DESIGN C: Using the Altera MAX+PLUSII CAD software, implement design **A** using schematic entry. You may use the 7476 device primitive and any necessary NAND devices in your schematic design. Simulate your design to verify its functionality. Print and turn in a copy of your schematic design (*.gdf) and simulation (*.scf) files.

DESIGN D: Using the Altera MAX+PLUSII CAD software, implement design **B** using schematic entry. You may use the 7476 device primitive and any necessary NAND devices in your schematic design. Simulate your design to verify its functionality. Print and turn in a copy of your schematic design (*.gdf) and simulation (*.scf) files.