The exam will be closed book and closed notes. The following questions are representative of the type of questions that will be on the exam. The exam will cover the lectures 12 and 14-26 from the class notes. A sheet showing Boolean theorems will be provided. There will be fifteen problems on the exam: 10 multiple choice (similar to samples 1-11) and 5 written (similar to samples 12-18).

1. Which of the following is the correct truth table for the tri-state buffer shown below:

   ![Tri-state buffer diagram]

   a) | e x f | b) | e x f | c) | e x f | d) | e x f |
   --|--|--|--|--|--|--|--|
     0 0 Z | 0 0 Z | 0 0 0 | 0 0 1 |
     0 1 Z | 0 1 Z | 0 1 0 | 0 1 1 |
     1 0 1 | 1 0 0 | 1 0 Z | 1 0 Z |
     1 1 1 | 1 1 0 | 1 1 Z | 1 1 Z |

   NONE

2. Convert \((A3)_{16}\) to octal.
   a) \((243)_8\)
   b) \((123)_8\)
   c) \((223)_8\)
   d) \((33)_8\)
   e) none of the above

3. The unsigned number \((1111101)_2\) is equal to which of the following?
   a) \((175)_{10}\)
   b) \((7D)_{16}\)
   c) \((175)_8\)
   d) Both a and b
   e) Both a and c

4. Convert \((78)_{10}\) the 8-bit 2’ complement binary representation.
   a) \((01001110)_2\)
   b) \((10111110)_2\)
   c) \((00110001)_2\)
   d) \((10111111)_2\)
   e) none of the above

5. What value is represented by the following 32-bit IEEE single precision floating point number?
   \(10111111110100000000000000000000\)
   a) \((0.8125)_{10}\)
   b) \((-0.8125)_{10}\)
   c) \((1.625)_{10}\)
   d) \((-1.625)_{10}\)
   e) none of the above
6. Which of the following is the correct truth table for the circuit shown below:

\[\begin{array}{cccc|c}
 x & y & z & f \\
 0 & 0 & 0 & 0 \\
 0 & 0 & 1 & 0 \\
 0 & 1 & 0 & 1 \\
 0 & 1 & 1 & 1 \\
 1 & 0 & 0 & 1 \\
 1 & 0 & 1 & 0 \\
 1 & 1 & 0 & 1 \\
 1 & 1 & 1 & 1 \\
\end{array}\]

Which circuit below implements the function \(f(x,y,z)=xy+xz+yz\)?

7. Which circuit below implements the function \(f(x,y,z)=xy+xz+yz\)?

8. Which of the following is the correct truth table for a JK flip-flop?

\[\begin{array}{ccc|c}
 J & K & Q(t+1) \\
 0 & 0 & Q(t) \\
 0 & 1 & 0 \\
 1 & 0 & 1 \\
 1 & 1 & X \\
\end{array}\]
9. Which of the following is the correct truth table for the gated SR latch circuit shown?

![Gated SR latch circuit diagram]

<table>
<thead>
<tr>
<th></th>
<th>Clk</th>
<th>S</th>
<th>R</th>
<th>Q(t+1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Q(t)</td>
</tr>
<tr>
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<td>0</td>
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<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Q(t)</td>
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<tr>
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<td>1</td>
<td>1</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

10. Which of the following statements is false?

a) A binary decoder has n inputs and $2^n$ outputs.
b) A binary encoder has $2^n$ inputs and n outputs.
c) A 74138 is a 3-to-8 decoder
d) A demultiplexer is the same circuit as an encoder.
e) None of the above

11. The timing diagram below shows the function of which of the following?

![Timing diagram]

<table>
<thead>
<tr>
<th></th>
<th>Clk</th>
<th>S</th>
<th>R</th>
<th>Q(t+1)</th>
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<tr>
<td></td>
<td>t_1</td>
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<td></td>
<td>t_2</td>
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<td></td>
<td>t_3</td>
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<td>t_4</td>
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</table>

a) A gated D latch
b) A positive edge triggered D-type flip-flop
c) A negative edge triggered D-type flip-flop
d) All of the above
e) None of the above
12. Write the behavioral VHDL code for a 32-bit adder.

```vhdl
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.numeric_std.all; -- provides arithmetic functions for vectors
ENTITY adder32 IS
PORT ( X, Y : IN  UNSIGNED(31 DOWNTO 0);
      S    : OUT UNSIGNED(31 DOWNTO 0));
END adder32;
ARCHITECTURE Behavior OF adder32 IS
BEGIN
  S <= X + Y;
END Behavior;
```

13. Give the VHDL architecture construct for a 2-bit priority encoder. Use a PROCESS statement in your description.

```vhdl
LIBRARY ieee;
USE ieee.std_logic_1164.all;
ENTITY priority IS
PORT ( w : IN  STD_LOGIC_VECTOR(3 DOWNTO 0);
       y : OUT STD_LOGIC_VECTOR(1 DOWNTO 0);
       z : OUT STD_LOGIC );
END priority;
ARCHITECTURE Behavior OF priority IS
BEGIN
  PROCESS ( w )
  BEGIN
    IF w(3) = '1' THEN
      y <= "11" ;
    ELSIF w(2) = '1' THEN
      y <= "10" ;
    ELSIF w(1) = '1' THEN
      y <= "01" ;
    ELSE
      y <= "00" ;
    END IF ;
  END PROCESS ;
  z <= '0' WHEN w = "0000" ELSE '1';
END Behavior ;
```

14. Write and explain the expression for the carry-output of a 4-bit carry lookahead adder.
15. Complete the given timing diagram for the circuit shown below.

![Timing diagram for JK flip-flop](image)

16. Add the following 8-bit 2'complement numbers.

\[(11001100)_2 + (01110011)_2\]

a) What is the 8-bit sum?
b) Is there an overflow?
c) What is the carry-output?

\[
\begin{array}{c}
11000000 \\
11001100 \\
01110011 \\
00111111 \\
\end{array}
\]

a) SUM=00111111B
b) No overflow
c) Carry output=1
17. Analyze the following counter circuit to determine the count sequence for the circuit.

![Counter Circuit Diagram]

<table>
<thead>
<tr>
<th></th>
<th>Q2</th>
<th>Q1</th>
<th>Q0</th>
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<tbody>
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18. Convert the following to a NAND-only multilevel circuit. Do not simplify.

![Multilevel Circuit Diagram]