ECE380 Digital Logic

Implementation Technology:
Standard Chips and
Programmable Logic Devices

Standard chips

- A number of chips, each with a few logic gates, are commonly used for small logic circuits
- These are known as 7400-series devices because the part numbers always begin with the number 74
  - Commonly packaged in a dual-inline package (DIP)
  - Chips external connections are called pins or leads
  - Two pins connect $V_{dd}$ and GND to supply power for the chip.
A 7400-series chip

Implementation of $f=ab+b'c$
7400-series chips

- For each specific 7400-series chip, a number of variants are fabricated with differing technologies
- For example:
  - The 74LS00 is built with a technology called transistor-transistor logic (TTL)
  - The 74HC00 is fabricated using CMOS technology
- Most popular chips in use today are the CMOS variants

Programmable logic devices

- The function provided by each 7400-series device is fixed and each chip only provides a few logic gates
  - These limitations make use of these chips inefficient for building large circuits
- It is possible to fabricate chips with a large amount of circuitry (gates) but with a structure (interconnection) that is not fixed
  - Called *programmable logic devices* (PLDs)
Programmable logic devices

- A PLD is a general purpose chip for implementing logic circuitry
- Contains a collection of logic circuit elements that can be customized in different ways
- Can be viewed as a black box containing logic gates and programmable switches that allow for different connections between the logic elements
- Can implement whatever logic circuit is needed – subject to limitations of the device

Programmable Logic Array (PLA)

- The first PLD developed was the **programmable logic array** (PLA)
- Based on the premise that any function can be written in SOP form, a PLA consists of
  - Input buffers and inverters that provide the true and complement form for each input variable
  - A collection of AND gates, with inputs that are selectable (programmable)
  - A collection of OR gates, with inputs that are selectable (programmable)
Gate-level diagram of a PLA

- OR plane
- AND plane
- Programmable connections

Customary schematic of a PLA

- OR plane
- AND plane

\[ f_1 = x_1x_2 + x_1x_3' + x_1'x_2'x_3 \]
\[ f_2 = x_1x_2 + x_1'x_2'x_3 + x_1x_3 \]
Programmable Array Logic (PAL)

• In a PLA both the AND and the OR planes are programmable
• A simpler device with a fixed OR plane is called a programmable array logic (PAL) device
  – As PALs are easier to manufacture and can operate faster than a PLA, most practical applications using these small programmable devices use the PAL structure

An example of a PAL

[Diagram showing a PAL with inputs X1, X2, X3, and outputs P1, P2, P3, P4, with functions f1 and f2.]
Extra circuitry in a PAL

- Most actual PAL devices include extra circuitry at the output of each OR gate to provide additional functionality.
- The term *macrocell* refers to the OR gate combined with the extra circuitry.

Complex Programmable Logic Devices (CPLDs)

- For larger designs that single PLAs or PALs cannot accommodate, a complex programmable logic device (CPLD) can be utilized.
- A CPLD consists of multiple circuit blocks with internal wiring to connect the blocks together and to the pins on the chip.
- Each circuit block is similar to a PAL.
  - PAL-like blocks.
- Commercial CPLDs have from 2 to more than 100 PAL-like blocks, with 16 macrocells in each block.
  - Each macrocell is the equivalent of approximately 20 gates.
  - About 20,000 equivalent gates in a CPLD of 1000 macrocells.
- Can construct moderately large logic circuits in a single chip.
### Structure of a CPLD

- Interconnection wires
- PAL-like block
- I/O block

### Field Programmable Gate Arrays

- To implement even larger circuits, it is convenient to use a different chip that has an even larger logic capacity
  - A field programmable gate array (FPGA)
- Does not contain AND and OR planes
  - Instead provides an array of logic blocks and interconnection wires between the logic blocks
  - Interconnection wires are arranged in horizontal and vertical routing channels containing wires are programmable switches
- Capable of implementing logic functions of millions of equivalent gates
Structure of an FPGA

- Logic block
- Interconnection switches

I/O block