ECE480/580 Digital Systems Design
Lab 4: Memory-Based Design
with Seven Segment Display Output

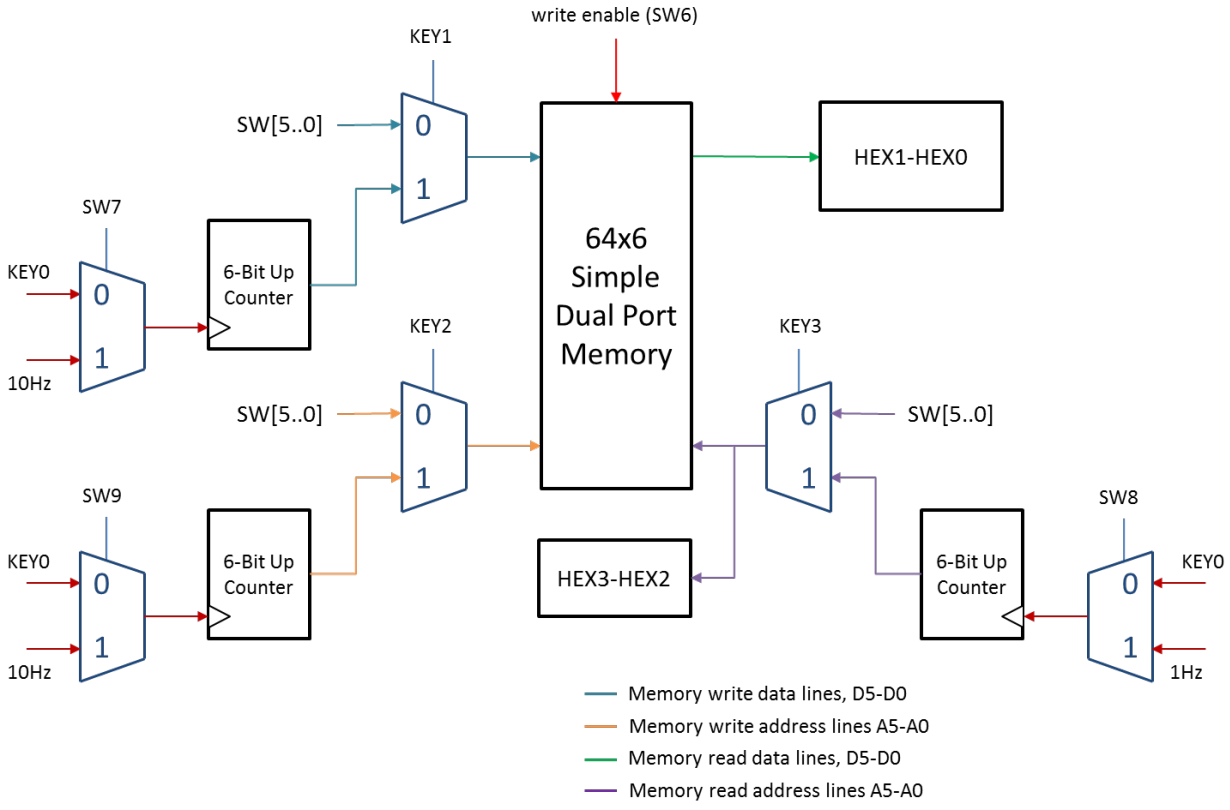
1. INTRODUCTION

In this lab, you will use the QUARTUS software package to design and simulate a memory-based design that output values to the seven segment displays. The requirements for this lab consist of completing QUARTUS designs and printing the VHDL files, functional simulation waveforms and laboratory report. Additionally, each design will require appropriate information obtained from various compilation reports and netlist viewers. All simulations should be done using the ModelSim-Altera Simulator. You may only use VHDL testbenches or ModelSim DO files to control the simulation.

2. DESIGN

Dual Port Memory System with Seven Segment Display Output

Design a system to display the content of a 64x6 dual port RAM to the seven segment display. A block diagram showing the system is given below.



Input data for writing to the memory is to be selectable (using KEY1) from either SW[5..0] or from a 6-bit up counter. The 6-bit data up counter is to be clocked from KEY0 or from a 10 Hz clock source (using SW7 to select the clock source). An input address for selecting a memory location to write is to be selectable (using

KEY2) from either SW[5..0] or from a 6-bit up counter. The 6-bit input address up counter is to be clocked from KEY0 or from a 10 Hz clock source (using SW9 to select the clock source).

An output address for selecting a memory location to read is to be selectable (using KEY3) from either SW[5..0] or from a 6-bit up counter. The 6-bit output address up counter is to be clocked from KEY0 or from a 1 Hz clock source (using SW8 to select the clock source). The selected output address is to be displayed on seven segment displays HEX3-HEX2. Data read from the output address should be displayed on seven segment displays HEX1-HEX0.

Clock inputs for the memory are to be defined by the designer. Carefully consider the memory clock requirements before implementing your design. Design options include clock frequency choice and separate versus single input and output clock sources.

The memory should be initialized with values 0x00-0x3F using a MIF file.

Include a ModelSim simulation that shows the output of at least the first eight memory location values to the seven segment display. Include all reports as in the previous labs in your lab report. Download your design to the Altera development board and test.