1. A Moore model finite state machine that acts as a “1011” sequence detector is to be designed using behavioral VHDL. Your design should detect overlapping sequences. Assume the input is named $A$, the output is named $Z$ and that an active low reset signal ($\text{reset}_n$) asynchronously resets the machine. The VHDL ENTITY construct is given. Write the corresponding VHDL ARCHITECTURE construct to implement the FSM. Implement positive edge triggered flip-flops.

(a) Draw the Moore model state diagram for the FSM.

(b) Write the VHDL ARCHITECTURE construct to implement the FSM.

library ieee;
use ieee.std_logic_1164.all;

entity seqdetect_fsm is
port (A  : in std_logic;
    clk   : in std_logic;
    reset_n : in std_logic;
    Z   : out std_logic);
end seqdetect_fsm;

2. Write a behavioral VHDL description for a 4-bit shift register. The shift register is to be negative edge triggered. $\text{Sin}$ is a serial input to the most significant bit of the shift register. $\text{Sout}$ is a serial output from the least significant bit of the shift register. $\text{En}_n$ is an active low enable. $\text{sreg}$ is the 4-bit register. Write only the VHDL ARCHITECTURE construct. The VHDL ENTITY construct is given below.

library ieee;
use ieee.std_logic_1164.all;

entity shiftreg is
port (  clk  : in std_logic;
    En_n  : in std_logic;
    Sin  : in std_logic;
    Sout  : out std_logic);
end shiftreg;

architecture behavior of shiftreg is
signal sreg  : std_logic_vector(3 downto 0);
begin
3. A given FPGA uses 2-input lookup tables to implement Boolean functions. Show a section of a programmed FPGA that implements the function $f(x,y,z)=\Sigma m(0,1,2,5,7)$.

4. Draw a diagram for typical output circuitry in a PLA. Describe each component.

5. What is the purpose of a sensitivity list in a VHDL PROCESS block?

6. Give the VHDL statement to implement the logic function in problem 3 using a selected assignment statement. Define any signals used in the statement.
Write a behavioral VHDL description for a 2-to-1 multiplexer. Model the multiplexer as a process block. Write only the VHDL ARCHITECTURE construct. The VHDL ENTITY construct is given below.

```vhdl
library ieee;
use ieee.std_logic_1164.all;

entity mux2to1 is
  port ( w : in std_logic_vector(1 downto 0);
         f : out std_logic);
end mux2to1;
```