ECE481/581 Digital Systems Design
Project II: Integrating the DE Processor with Video Display

1. INTRODUCTION

For this project, you will integrate your previously designed DE computer and a video display. The design will include a text display of appropriate DE processor registers, instruction execution, and DE board status information. The design will also include a graphics-based video display with object motion controlled by the assembly language program executing on your DE processor.

The requirements for this project consist of completing the design and printing the source files, waveform displays from simulation and the SignalTap Logic Analyzer, and project report. Additionally, the report should include appropriate information obtained from various compilation reports and netlist viewers.

2. DESIGN

The VGA display resolution is to be 800x600 pixels with a 12-bit/pixel color resolution. The monitor refresh rate is to be 60 Hz. The screen is to be separated into two fields. The upper field will be used for text display and should support ten (10) rows of 8x8 characters. Minimally, the text field is to display contents of MAR, MDR, PC, IR, R[0], and R[1] registers. The text field is also to display the values of all switches and pushbuttons on the DE board. Optionally, the text field is to display the assembly language mnemonic for the currently executing instruction.

The graphics field is devoted to the display of graphics objects whose motion is controlled by the program executing on the DE processor. Minimally, your design must show the display of a single object that moves throughout the portion of the video display devoted to graphics. The data for the object to display should be provided by an appropriate RAM or ROM. Object motion is to be controlled by the program executing on the DE processor. Your program should exercise all reasonable ranges of motion of the object to be displayed.

There are to be two clock sources for your computer. If SW[9]=0 then the clock source for the computer is to be the output of a PLL. The PLL output frequency should be a minimum of 100 MHz. If SW[9]=1, the clock source is to be the KEY[0] pushbutton.

Create a SignalTap II Logic Analyzer instance and verify your design as it operates. Display sufficient signals to verify your design. Generate an appropriate sampling clock from a PLL source.

View the compilation report files (*.rpt) that are generated when you compile your design. Summarize LE, memory, and interconnect usage for your design. After the design is finalized, print the device floorplan showing LE, memory, and pin usage. Print the top level hierarchy shown in both the RTL Viewer and the Technology Map Viewer and include in your report. Download your design to the Altera development board and test.