Digital Systems Design

Programmable Device Technologies and Introduction to the Altera Cyclone V FPGA

Programmable Logic Device Black Box
General PLA Structure

Input buffers and inverters

AND plane

OR plane

Programmable connections

Gate Level PLA Structure
Customary Schematic of a PLA

AND plane

OR plane

P1
P2
P3
P4
f1
f2

Typical PLA Output Circuitry

Select
Enable

Flip-flop

D
Q

Clock

f1

To AND plane
**Structure of a CPLD**

- PAL-like block
- I/O block
- Interconnection wires

**A Section of a CPLD**

- PAL-like block (details not shown)
- Interconnection wires
VHDL code for the function $f = \sum m(0,2,4,5,6)$

```vhdl
library ieee;
use ieee.std_logic_1164.all;

entity func3 is
port ( x1, x2, x3 : in std_logic;
       f       : out std_logic);
end func3;

architecture logicfunc of func3 is
begin
  f <= (not x1 and not x2 and not x3) or
       (not x1 and x2 and not x3) or
       (x1 and not x2 and not x3) or
       (x1 and not x2 and x3) or
       (x1 and x2 and not x3);
end logicfunc;
```

VHDL Implementation of $f = \sum m(0,2,4,5,6)$

(from interconnection wires)

```
```

(x1, x2, x3, unused) to PAL-like block
Structure of an FPGA

- Logic block
- Interconnection switches
- I/O block

A Two-Input Lookup Table

(a) Circuit for a two-input LUT

(b) $f_1 = x_1 \cdot x_2$

(c) Storage cell contents in the LUT
A Three-Input Lookup Table

Inclusion of a flip-flop With an LUT
A Section of a Programmed FPGA

Pass transistor Switches in an FPGA

(to other wires)
Cyclone V General Features

- Contain a two-dimensional row- and column-based architecture to implement custom logic
- Column and row interconnects of varying speeds provide signal interconnects between logic array blocks (LABs)
- The logic array consists of LABs, with 10 adaptive logic modules (ALMs) in each LAB
  - An ALM is a small unit of logic providing efficient implementation of user logic functions
  - LABs are grouped into rows and columns across the device

Cyclone V General Features

- The LAB is composed of basic building blocks known as adaptive logic modules (ALMs) that you can configure to implement logic functions, arithmetic functions, and register functions
- You can use a quarter of the available LABs in Cyclone V devices as a memory LAB (MLAB)
  - Each MLAB supports a maximum of 640 bits of simple dual-port SRAM
  - You can configure each ALM in an MLAB as a 32 x 2 memory block, resulting in a configuration of 32 x 20 simple dual-port SRAM blocks
LAB Structure and Interconnects
Overview in Cyclone V Devices

High-Level Block Diagram of the Cyclone V ALM
ALM Registers

- One ALM contains four programmable registers. Each register has data, clock, synchronous and asynchronous clear, and synchronous load functions
- Global signals, general-purpose I/O (GPIO) pins, or any internal logic can drive the clock and clear control signals of an ALM register
- GPIO pins or internal logic drives the clock enable signal
- For combinational functions, the registers are bypassed and the output of the look-up table (LUT) drives directly to the outputs of an ALM

Memory Blocks in Cyclone V Devices

- The Cyclone V devices contain two types of memory blocks
  - M10K blocks—10-kilobit (Kb) blocks of dedicated memory resources that you can use to create designs with large memory configurations
  - Memory logic array blocks (MLABs)—640-bit enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs)
    - The MLABs are optimized for implementation of shift registers and other similar logic
Memory Modes Supported in the Memory Blocks

- Single-port RAM
- Simple dual-port RAM
- True dual-port RAM
- Shift Register
- ROM
- FIFO Buffer

Cyclone V Device Packaging Information

- Package Type
  - F: FineLine BGA (FBGA)
  - U: Ultra FineLine BGA (UBGA)
  - M: Micro FineLine BGA (UMBG)
- Operating Temperature
  - C: Commercial (Tj = -0°C to 85°C)
  - I: Industrial (Tj = -40°C to 100°C)
  - A: Automotive (Tj = -40°C to 125°C)
- Optional Suffix
  - Indicates specific device options or shipment method
  - N: Lead-free packaging
  - Contact Altera for availability of loaded options
  - E: Engineering sample
  - SC: Internal scrubbing support

- Embedded Hard IPs
  - E: No hard PLD or hard memory controller
  - F: No hard PLD and maximum 2 hard memory controllers

- Family Signature
  - SC: Cyclone V

- Family Variant
  - E: Enhanced logic/memory

- Member Code
  - A2: 25K logic elements
  - A4: 40K logic elements
  - A5: 77K logic elements
  - A7: 150K logic elements
  - A9: 300K logic elements

- Package Code
  - FBGA Package Type
    - 17: 256 pins
    - 23: 404 pins
    - 27: 572 pins
    - 31: 896 pins
  - EBG Package Type
    - 15: 334 pins
    - 19: 484 pins
    - MBGA Package Type
      - 13: 383 pins
      - 15: 484 pins

- FPGA Fabric Speed Grade
  - 6 (fastest)
  - 7
  - 8
## Maximum Resource Counts for Cyclone V E Devices

<table>
<thead>
<tr>
<th>Resource</th>
<th>A2</th>
<th>A4</th>
<th>A5</th>
<th>A7</th>
<th>A9</th>
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<tbody>
<tr>
<td>Logic Elements (LE) (K)</td>
<td>25</td>
<td>49</td>
<td>77</td>
<td>150</td>
<td>301</td>
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<tr>
<td>ALM</td>
<td>9,434</td>
<td>18,480</td>
<td>29,080</td>
<td>56,480</td>
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<td>Register</td>
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<td>116,320</td>
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<tr>
<td>Memory (Kb)</td>
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<td>4,460</td>
<td>6,860</td>
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<td>M10X</td>
<td>196</td>
<td>303</td>
<td>424</td>
<td>836</td>
<td>1,717</td>
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<tr>
<td>MLAB</td>
<td>25</td>
<td>66</td>
<td>150</td>
<td>156</td>
<td>342</td>
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<tr>
<td>Variable-precision DSP Block</td>
<td>50</td>
<td>132</td>
<td>300</td>
<td>312</td>
<td>684</td>
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<td>18 x 18 Multiplier</td>
<td>4</td>
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<td>6</td>
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<td>8</td>
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<td>PLL</td>
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<td>224</td>
<td>240</td>
<td>480</td>
<td>480</td>
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<td>LVDS Transmitter</td>
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<td>120</td>
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<tr>
<td>LVDS Receiver</td>
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<td>56</td>
<td>60</td>
<td>120</td>
<td>120</td>
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<tr>
<td>Hard Memory Controller</td>
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<td>1</td>
<td>2</td>
<td>2</td>
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